Novel organic chip packaging technology and impacts on high speed interfaces

Novel Organic Chip Packaging Technology and Impacts on High Speed Interfaces

Bernd Garben, Andreas Huber, Dierk Kaller, Erich Klink, IBM Deutschland Entwicklung GmbH,
7032 Boeblingen , Email: garbenb@de.ibm.com, huber@de.ibm.com, Kaller@de.ibm.com,
eklink@de.ibm.com, Phone: 49-7031-16-2590, Fax: 49-7031-16-2042
Stefano Grivet-Talocia, Dipartimento di Elettronica, Politecnico di Torino,
C.Duca degli Abruzzi 24, 10129, Torino, Italia, Email: grivet@polito.it,
George A. Katopis, IBM Laboratory, Poughkeepsie, NY, Email: katopis@us.ibm.com,

Abstract

The high dense interconnect (HDI) organic chip packaging technology has made rapid development advancements in the last few years. Due to the dense wiring structures in the build up layers and newly also in the laminated core, high signal I/O applications and dense chip area array footprints can be supported. These technology improvements allow specific applications. In this paper the electrical characteristics of the HDI organic chip packaging technology are described with regards to signal and power noise. In addition the impact on high speed data transmission and the performance differences between single-chip module (SCM) and multi-chip modules (MCM) are discussed.

Introduction

The evolution of the high dense interconnect organic chip packaging technology has taken very fast development steps during the last eight years and a similar rapid advancement can be predicted for the near future. The standard card & board technology, used as chip carrier, is generally viewed as the first generation. The first generation was only capable to support wire bonded chips with very low signal I/O counts. The invention of build up layers with micro via-holes in 1992 at both sides of the laminated core, enabled this technology to facilitate also flip chip applications with modest signal I/O counts. This technology is considered as the second generation (GEN 2).

The third generation (GEN 3) of the organic chip carrier technology shows a significant progress due the development of the fine line core technology. Table 1 shows the key factors of the technology roadmap spanning from the GEN 2 to GEN 3 into the predicted future generation. One key factor is the line width of the build up layers and core layers (w - in Fig.1) and the second important factor is the via land size (V2 in Fig.1). Table 1 shows the improvements in line width and the reduction of the core via land, which is the main achievement factor of generation 3, obtained due to the development of the fine line core technology. Fig. 1 depicts the standard organic chip carrier technology of the second generation (GEN 2). The cross section describes a 2-2-2 structure. This means that two build up layers on top and two build up layers on bottom are applied on a two layer laminated core.

The third generation (GEN 3) solves the disadvantage that the high wiring capabilities of the build up layers are not any more disturbed or even "disconnected" by the coarse core ground rules. The large core via land size (V) blocked the connectivity between the wiring in the top build up layers with the wiring in the bottom build up layers. Generation 3 has achieved similar ground rules for core as for build up layers. This enables the third generation to support very high signal I/O counts with more than 1000 signals per chip. In addition also small multi-chip modules can be wired and some applications will be shown in this paper.

Packaging applications

With the introduction of GEN 3 the applications are extended to high I/O single chip modules with very dense area array flip chip footprints. These chip footprints will have bump pitches below 200 µm. Figure 2 shows such a typical SCM application. The single chip module can consist out of a multi-layer fine line core with or without build up layers on top and bottom side of the core. The off-module connections are usually provided with solder ball connects but can also be performed by pins.

Due to the high wiring capabilities multi-chip module applications can also be supported. The classical multi-chip module is realized by assembling two chips side by side close to each other on the top side of the module as shown in lower part of Figure 3. A typical MCM application can consist out of the processor chip (CP) and its private L2 cache chip. Figure 3 also shows the data path comparison from CP to L2 for SCM vs. MCM applications. For the SCM application the typical data path lengths are in the range of 10 mm on SCM and 70 mm on card, while for the MCM application the data path is typically realized by 40 mm of on MCM wiring.

A very high dense and extremely short CP-L2 data path is shown in Figure 4. In this specific multi-chip module application the cavity in the core is used for the back side mounted L2 cache chip. Due to the dense vertical structure, the chip to chip signal and power connections are basically only stacked via-

0-7803-7451-7/02/$17.00 © 2002 IEEE

holes through the build up layers or fine line core layers. The very short data path supports the CP-L2 interface performance at processor cycle.

The high number of signals in conjunction with the fast cycle time leads to a very high CP-L2 bandwidth. This specific double sided structure requires that the chip footprints of the CP and L2 chip have to be optimized together. The high number of Voltage & GND bumps and MCM via-holes also help to achieve a single sided cooling system.

Electrical characteristics

Table 2 summarizes the trend of the key electrical parameters. The values of the dielectric constant reduce from 4.0 of today's build up layer and core materials to 3.0 in the near future. In addition the dielectric loss decreases by a factor of ten from 0.03 to the very low value of 0.003 for future core materials. The impedance of the build up layers is below 50 Ohm for the second generation (GEN 2) and will increase to 50 Ohm. The impedance of the core layers is at 50 Ohm today and increases to values above 50 Ohm. It has to be emphasized that the characteristic impedance varies because of the decreasing spacing between lines. The coupling between adjacent lines increases continuously due to denser wiring. The saturated near end cross talk (NEXT) values in table 2 demonstrate this tendency. This behavior is similar to the on-chip wiring development, described in [2]. The maximum routing lengths are increasingly determined by cross talk effects.

Figure 5 depicts the cross talk analysis of an on-MCM line pair with a parallel line length of 40 mm. The voltage curves of near end (NE) and far end (FE) noise are shown for build up and core layers. The active line is connected to a 50 Ohm driver with a signal rise time of 100 ps and 500 mV swing.

The results show that the near end (NE) and far end (FE) coupled noise values increase through the generations, because of the significant higher wiring density as shown in Table 2. Although the coupled noise values are not high, they have to be carefully taken into account during system design. This is achieved with a detailed system timing and coupled noise analysis including all coupling segments along the lines. To guarantee accuracy the transmission line models and the simulation algorithm must account for frequency dependent parameters.

The parallel line length of 40 mm is a typical value valid for small multi-chip modules. For single-chip modules however the dense parallel line length is significantly shorter (ca. 10 mm).

Figure 6 compares the transmission eye for on MCM nets vs. SCM-SCM nets (as described in Fig.3) using a single rail (not differential) signal transmission scheme including coupling of one neighbor line. To achieve a secure signal transmission from the driver to the receiver, the criteria for the opening of the signal transmission eye is a minimum of the half bit time. This means for a bit time of 100 ps (10 Gbps) an opening of 50 ps is needed. The vertical height for this eye is defined by the used receiver technology. It has to be noted that this criteria does not define the highest possible transmission frequency for the transmission channel, but is used as a simplified standard rule. There exist additional circuit methodologies for high speed data transmission, such as driver predistortion, channel equalization, coupled noise cancellation etc., which increase the channel bandwidth. However these methods are not described in this paper. Fig. 6 shows that the eye opening for on-MCM nets are much larger than for the SCM to SCM nets. The eye opening of the MCM net is 45 ps, while the eye opening for the SCM to SCM net is only 12 ps applying the future BU technology.

In Table 3 the timing and noise simulation results for the eye opening are summarized for the BU technology generations with a cycle time of 100 ps. Due to increasing noise and especially increasing attenuation the eye opening decreases in general going to smaller line dimensions. In the MCM case the eye opening is significant larger than the SCM case due to much less disturbance and shorter net length as shown in Fig. 6. This means that the SCM-SCM nets are far away to meet the eye opening criteria.

Figure 7 and 8 describe the details of the mid frequency power noise analysis. Figure 7 shows the equivalent subcircuit model applied for the power noise analysis. The elements C1,R1 represent a portion of the on-chip decaps. The elements L2, C2, R2 represent a section of the on-module capacitors and L3,C3,R3 depict a portion of the on-card capacitors. The inductances L5,L6 are schematically inserted and describe the effective loop inductance of the V/GND planes and via-holes on the module and on the card, connecting to the on-module and on-card capacitors respectively. The resistances (r5,r6) and the capacitances (C5,C6) also belong to these planes. Actually the total power distribution network is modeled by a 3D field solver which supports EM wave propagation through the multi-layers. The current sources i(t) represent synchronously switching on-chip currents.

Figure 8 shows the results of the mid frequency power noise analysis comparing the technology of the first generation with the technology of the second generation. Due to the much lower effective V/GND loop inductance, which connects the on-module decaps to the chip, the power noise is significantly reduced by more than 40 % . The smaller effective loop inductance is achieved by the thin insulation

build up layer, which separates the voltage and the GND planes. As the dielectric thickness of the build up layers continues to decrease from generation 2 to generation 3, the mid frequency power noise is further reduced

Conclusions / Summary

The characteristics and benefits of the HDI organic chip packaging technology have been demonstrated. It has been shown that the third generation has superior characteristics with regards to wireability. Therefore large and dense chip footprints can be supported. This will lead to high signal I/O count single-chip and small multi-chip module applications.

The results of the electrical signal integrity analysis revealed cross talk values which are not very high, but they have to be controlled carefully during the system design. Together with the increased wireability, this gives significant bus performance advantages especially for MCM applications. The mid frequency power noise analysis displayed reduced noise values.

Acknowledgment

The authors would like to thank Edmund Blackshear from IBM Fishkill and Toshihiko Nishio from IBM Yasu for their helpful feedback and discussions.

References

[1] Tummala, R. R., Microsystem Packaging, McGraw-Hill (New York, 2001), pp. 321. [packaging fundamentals ...]

[2] Winkel T.; Kaller D. ; Huber A.: "Determination of Critical Line Length for On-Chip Interconnects for the Future Technologies as predicted in the SIA Roadmap", 4th IEEE Workshop on Signal Propagation on Interconnects, 2000

	GEN 2	GEN 3	Future
Line width BU/core [µm]	65/75	30/30	20/25
Via land BU/core [µm]	150/500	70/150	55/80

Table 1:
Organic Chip carrier technology roadmap

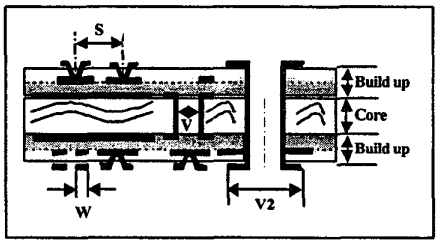

Figure 1: Organic chip carrier technology (2-2-2) Build up layers on laminated core

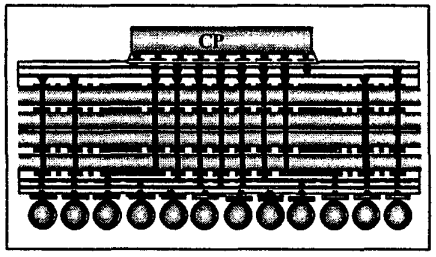

Figure 2: SCM application with fine line core technology and build up layers

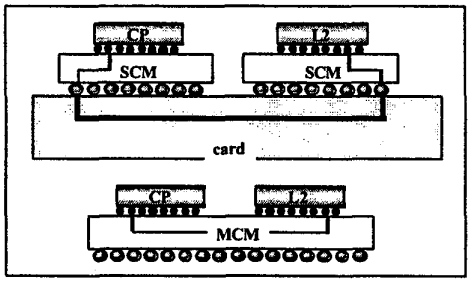

Figure 3:
Data path from CP-SCM to L2-SCM compared to on-MCM CP-L2 data path.

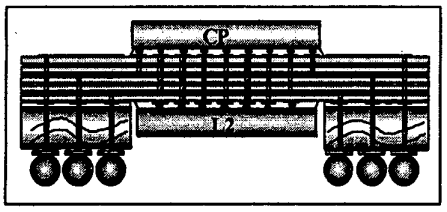

Figure 4: Double sided MCM application with fine line core technology. L2 cache chip embedded in core pocket on module back side

	GEN 2	GEN 3	Future
ε – BU/core	4.0	3.5	3.0
tan δ – BU/core	0.03/0.03	0.02/0.01	0.01/0.003
Z_0 BU/core [Ω]	40 / 50	50 / 50	50 / 55
NEXT BU/core	1 / 6 %	5.5 / 8 %	6.5 / 9 %

Table 2: Summary of key electrical parameter

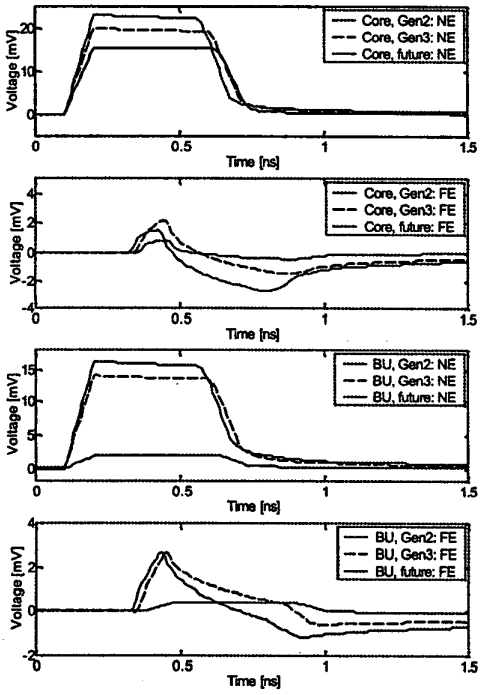

Figure 5: Comparison of near end (NE) and far end (FE) coupled noise of 40 mm parallel line pair in the core & BU layers

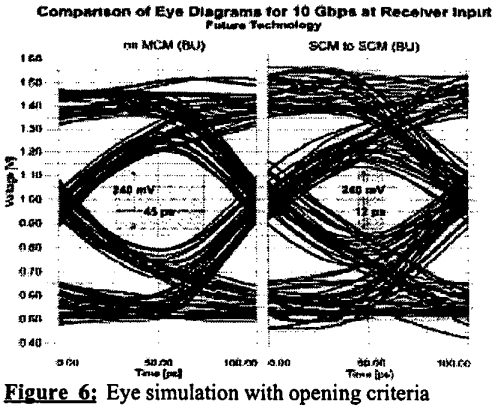

Figure 6: Eye simulation with opening criteria for secure signal transmission (min width = 50ps, min. amplitude = ±120 mV)

Eye opening	BU GEN 2	BU GEN 3	BU Future
On MCM	63 ps	49 ps	45 ps
SCM-SCM	44 ps	30 ps	12 ps

Table 3: Comparison of eye opening for 40mm MCM lines wired in BU layers at 10 Gbps.

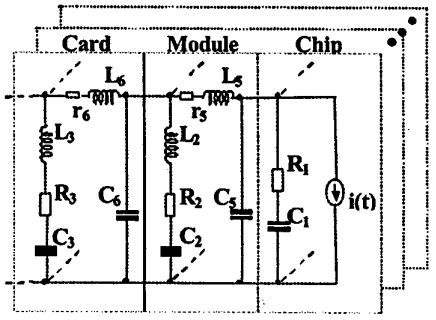

Figure 7: Equivalent subcircuit for mid frequency power noise analysis

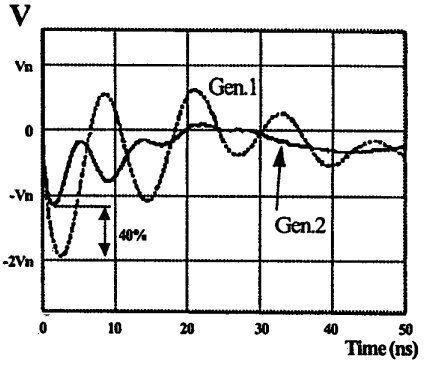

Figure 8: Mid frequency power noise analysis. Comparison of GEN 2/3 with GEN 1